IN THE CLAIMS

Claims 1-21 (Canceled)

22. (Currently Amended) The apparatus of claim ~~21~~ 27, wherein the programmable delay circuit comprises:

a plurality of the delay elements to generate a plurality of delayed clock signals;

a programmable register to store information indicating a particular delayed clock signal of the plurality of delayed clock signals; and

a multiplexer coupled with the programmable register and the plurality of delay elements to select the particular delayed clock signal based on the information.

23. (Currently Amended) ~~The apparatus of claim 22, wherein the programmable delay circuit further comprises~~ An apparatus, comprising:

a content addressable memory (CAM) array;

a clocked circuit coupled to the CAM array; and

a programmable delay circuit coupled to receive a reference clock signal and generate a programmable delayed clock signal using a delay element for the clocked circuit, wherein the programmable delay circuit comprises:

a plurality of the delay elements to generate a plurality of delayed clock signals;

a programmable register to store information indicating a particular delayed clock signal of the plurality of delayed clock signals;

a multiplexer coupled with the programmable register and the plurality of delay elements to select the particular delayed clock signal based on the information; and

a decoder coupled to the programmable register to decode the information stored in the programmable register.

24. (Currently Amended) The apparatus of claim ~~22~~ 23, wherein each of the plurality of delay elements provides a different time period of delay to the reference clock signal.

25. (Currently Amended) The apparatus of claim ~~21~~ 27, wherein the clocked circuit comprises a read circuit for reading data from the CAM array.

26. (Currently Amended) ~~The apparatus of claim 21,~~ An apparatus, comprising:

a content addressable memory (CAM) array;

a clocked circuit coupled to the CAM array; and

a programmable delay circuit coupled to receive a reference clock signal and generate a programmable delayed clock signal using a delay element for the clocked circuit, wherein the clocked circuit comprises a register for storing comparand data for comparison with data of the CAM array.

27. (Currently Amended) ~~The apparatus of claim 21,~~ An apparatus, comprising:

a content addressable memory (CAM) array;

a clocked circuit coupled to the CAM array; and

a programmable delay circuit coupled to receive a reference clock signal and generate a programmable delayed clock signal using a delay element for the clocked

circuit, wherein the CAM array comprises a plurality of rows of CAM cells each having a corresponding match line for carrying a match signal indicative of whether comparand data matches data of the corresponding row of CAM cells.

28. (Original) The apparatus of claim 27, wherein the clocked circuit comprises an encoder circuit coupled to the match lines and the programmable delay circuit.

29. (Original) The apparatus of claim 28, wherein the clocked circuit comprises match flag logic coupled to the match lines and the programmable delay circuit.

30. (Currently Amended) The apparatus of claim ~~21~~ 27, further comprising:

a second clocked circuit; and

a second programmable delay circuit.

Claims 31-53 (Canceled)